Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1 (currently amended). An electronic device, comprising:

an input for receiving successive data words, wherein each data word of the successive data words comprises a plurality of bits;

a memory structure comprising a plurality of memory word addresses, wherein each memory word address corresponds to a storage structure operable to store a data word having the plurality of bits;

control circuitry, operable during a non-overflow condition of the memory structure, for writing successive ones of received data words into respective successive ones of the memory word addresses; and

control circuitry, operable during an overflow condition of the memory structure, for writing each data word, in successive ones of received data words, across multiple ones of the memory word addresses.

2 (original). The electronic device of claim 1 wherein the control circuitry, operable during an overflow condition of the memory structure, is for writing each data word in the successive ones of received data words across a same set of the multiple ones of the memory word addresses.

3 (original). The electronic device of claim 2:

wherein the plurality of bits consists of an integer number *N* of bits; and

wherein *N* is selected from a group consisting of 128, 64, 32, 16, 8, and 4.

4 (original). The electronic device of claim 1 wherein the control circuitry, operable during an overflow condition of the memory structure, is for writing each data word in the successive ones of received data words across a same set of multiple contiguously-addressed ones of the memory word addresses.

5 (original). The electronic device of claim 1 and further comprising circuitry for detecting the overflow condition.

6 (original). The electronic device of claim 5 wherein the circuitry for detecting the overflow condition is responsive to detecting a potential write of a data word into one of the memory word addresses, wherein the one memory word address already stores an unread data word.

7 (original). The electronic device of claim 1 and further comprising circuitry for reading data words written during the non-overflow condition.

8 (original). The electronic device of claim 7 and further comprising circuitry for reading data words written during the overflow condition.

9 (original). The electronic device of claim 8 wherein the circuitry for reading data words written during the overflow condition comprises circuitry for reading each data word from multiple contiguously-addressed ones of the memory word addresses.

10 (original). The electronic device of claim 1 wherein the memory structure, the control circuitry operable during a non-overflow condition of the memory structure, and the control circuitry operable during an overflow condition are all part of a handheld computing device.

11 (original). The electronic device of claim 1 wherein the successive data words represent data selected from a group consisting of audio, screen trace, bit map, and uncompressed video data.

12 (currently amended). A method of operating an electronic device, the device comprising a memory structure comprising a plurality of memory word addresses, wherein each memory word address corresponds to a storage structure operable to store a data word having the plurality of bits, the method comprising:

receiving, at an input, successive data words, wherein each data word of the successive data words comprises a plurality of bits;

during a non-overflow condition of the memory structure, writing successive ones of received data words into respective successive ones of the memory word addresses; and

during an overflow condition of the memory structure, writing each data word, in successive ones of received data words, across multiple ones of the memory word addresses.

13 (original). The method of claim 13 wherein the writing step, during the overflow condition of the memory structure, comprises writing each data word in the successive ones of received data words across a same set of the multiple ones of the memory word addresses.

14 (original). The method of claim 13:

wherein the plurality of bits consists of an integer number *N* of bits; and

wherein *N* is selected from a group consisting of 128, 64, 32, 16, 8, and 4.

15 (original). The method of claim 12 wherein the writing step, operable during the overflow condition of the memory structure, comprises writing each data word in the successive ones of received data words across a same set of multiple contiguously-addressed ones of the memory word addresses.

16 (original). The method of claim 12 and further comprising detecting the overflow condition by detecting a potential write of a data word into one of the memory word addresses, wherein the one memory word address already stores an unread data word.

17 (original). The method of claim 12 and further comprising reading data words written during the non-overflow condition.

18 (original). The method of claim 17 and further comprising reading data words written during the overflow condition.

19 (original). The method of claim 18 wherein the step of reading data words written during the overflow condition comprises reading each data word from multiple contiguously-addressed ones of the memory word addresses.

20 (original). The method of claim 12 wherein the successive data words represent data selected from a group consisting of audio, screen trace, bit map, and uncompressed video data.